Docket No.: 050099-0355 **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|
| In re Application of | : | Customer Number: 20277 |
| Fukashi MORISHITA, et al. | : | Confirmation Number: Not Yet Assigned |
| Application No.: Not Yet Assigned | : | Group Art Unit: Not Yet Assigned |
| Filed: September 18, 2006 | : | Examiner: Not Yet Assigned |

For: SEMICONDUCTOR MEMORY DEVICE

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed with the application and no certification or fee is required.

A copy of the foreign search report is attached for the Examiner's information. Please note this is a PCT application in the entry of the National Phase in the U.S. and copies of the references cited were transmitted by WIPO and are believed to be in the file of the above identified application and readily available to the Examiner. Therefore it is believed that Applicants have met all requirements regarding duty of disclosure under 37

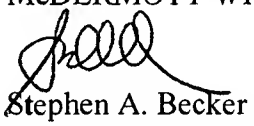
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.L./

CFR 1.56. Acknowledgement and consideration of these documents are respectfully requested.

Since the Search Report was from the JPO search authorities, copies of these references should have been supplied to the USPTO under the trilateral agreement and are believed to be in the file of the above identified application and readily available to the Examiner. However, to ensure that these references are available to the Examiner, we are providing copies of these references herewith.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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**Please recognize our Customer No. 20277 as our correspondence address.**

IAP12 Rec'd PCT/PTO 18 SEP 2006



# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

| ATTY. DOCKET NO. | SERIAL NO. |
|---|---|
| 050099-0355 | Not Yet Assigned 10/593275 |
| APPLICANT: Fukashi MORISHITA, et al. | |
| FILING DATE: September 18, 2006 | GROUP: Not Yet Assigned |

## U.S. PATENT DOCUMENTS

| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Code2 (if known) | | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | | US | 2002-0114191 A1 | 08/22/2002 | Iwata et al. | Corresponds to JP 2003-86712 |
| | | US | 6,204,534 | 03/20/2001 | Adan | Corresponds to JP 10-209456 |
| | | US | | | | |
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## FOREIGN PATENT DOCUMENTS

| EXAMINER'S INITIALS | CITE NO. | Foreign Patent Document Country Codes3-Number 4-Kind Codes (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines Where Relevant Figures Appear | Translation Yes | Translation No |
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| | | JP 2003-86712 | 03/20/2003 | TOSHIBA CORP | Corresponds to US 2002-0114191 A1 | | X |
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

| EXAMINER'S INITIALS | CITE NO. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | |
|---|---|---|---|
| | | Kuo, C., et al. "A Capacitorless Double Gate DRAM Technology for Sub-100-nm Embedded and Stand-Alone Memory Applications" IEEE Transactions of Electron Devices, December 2003, Vol. 50, No. 12, pp. 2408-2416. | |
| | | Kuo, C., et al. "A Capacitorless Double Gate Cell" IEEE Electron Device Letters, June 2002, Vol. 23, No. 6, pp. 345-347. | |
| | | Ohsawa, T., et al. "Memory Design Using One-Transistor Gain Cell on SOI" Digest of Technical Papers, IEEE International Solid-State Circuits Conference, February 5, 2002, pp. 152-153, 454-455. | |
| | | | |

| EXAMINER | DATE CONSIDERED |
|---|---|
| /Peter Loxas/ | 07/15/2009 |

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.L./